JULY 9–13, 2023

MOSCONE WEST CENTER

SAN FRANCISCO, CA, USA

GUC

Global Unichip Corporation

High Bandwidth Memory (HBM3-7.2Gbps) 2.5D-IC Integration with Signal Interconnects and Power Distributed Networks Design-Optimization

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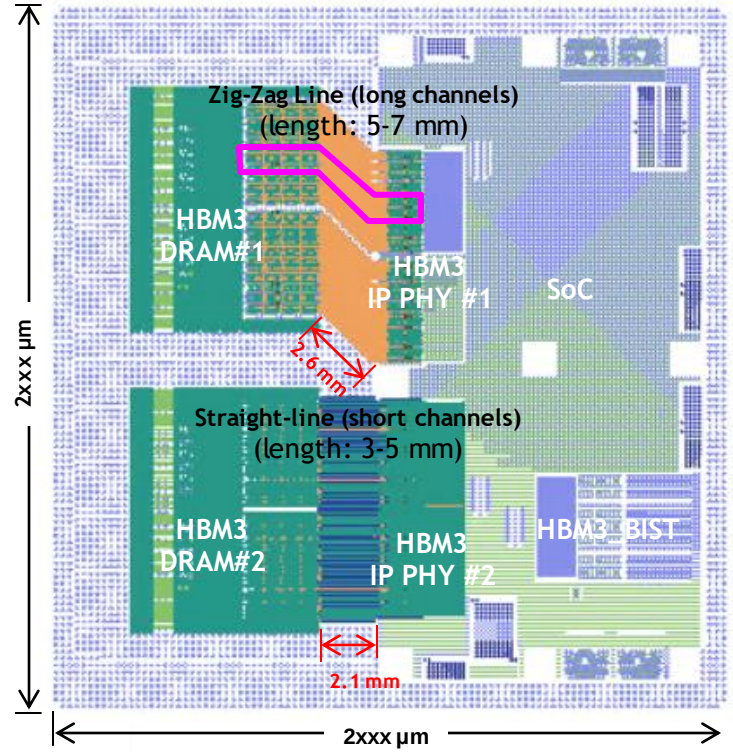
Motivation

- For 5G/AI and HPC applications, 2.5D-IC chiplets integration with high bandwidth memory (HBM) has been a critical demand in recent years. To achieve this demand, HBM3 was emerged in 2016. Its total data throughput can be up to 922GB/s with 7.2GT/s per data transmission lane, than that of HBM2E by 512GB/s with 4.0GT/s.
- This work presents an silicon proven HBM3 PHY IP chiplets integrated solution at CoWoS platforms. Its design-optimization consists of signal integrity at high speed silicon interposer interconnections (insertion loss less than 4.7dB) and power integrity at chip/interposer/package/board whole PDNs.
- This work is implemented by silicon technology of HBM3 IP PHY in 7nm, and CoWoS interposer in 65nm, where it can achieve HBM3-7.2Gbps with eyewidth to 0.52-0.68UI at CoWoS-S and 0.68-0.79UI at CoWoS-R, as well as maximum voltage drop (DC+AC) suppressed to less than 5% from supply voltages (both power domains, 0.4V and 0.75V).

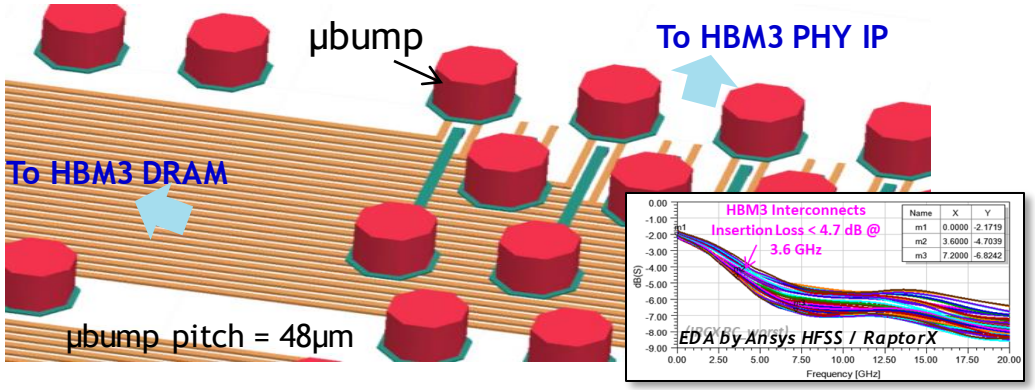
SI/PI Design-Optimization at CoWoS-S/-R

Chiplets Floorplan of HBM3 CoWoS-S/-R Interposer

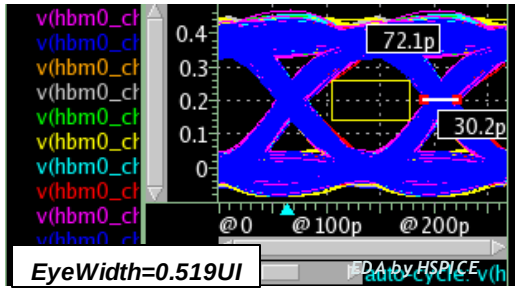


p.s., 65nm technology Silicon Interposer of CoWoS® (Chip on Wafer on Substrate).

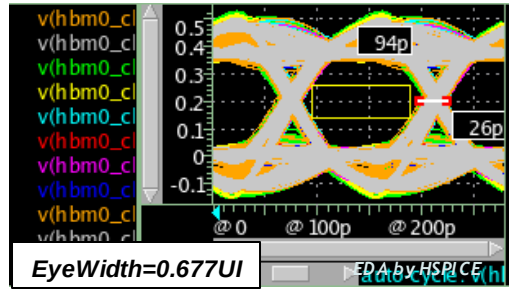
Silicon-interposer Fan-outs & High speed interconnects



Silicon Interposer, CoWoS-S
L/S= 2.5µm/2.5µm, SI-co-sim.

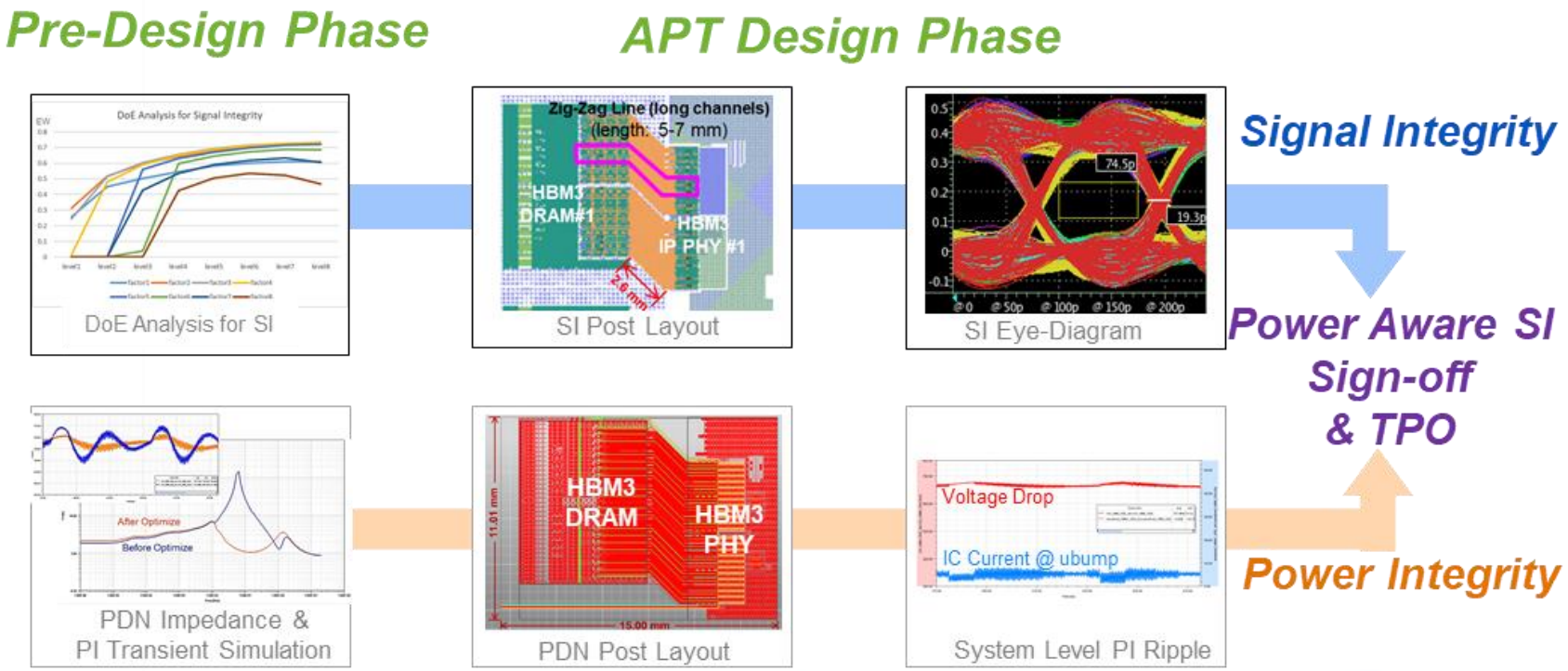


RDL Interposer, CoWoS-R
L/S = 2µm/2µm, SI-co-sim.

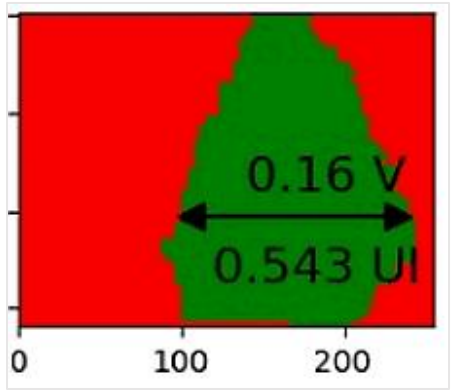


SI/PI Design-Optimization and Design Flow

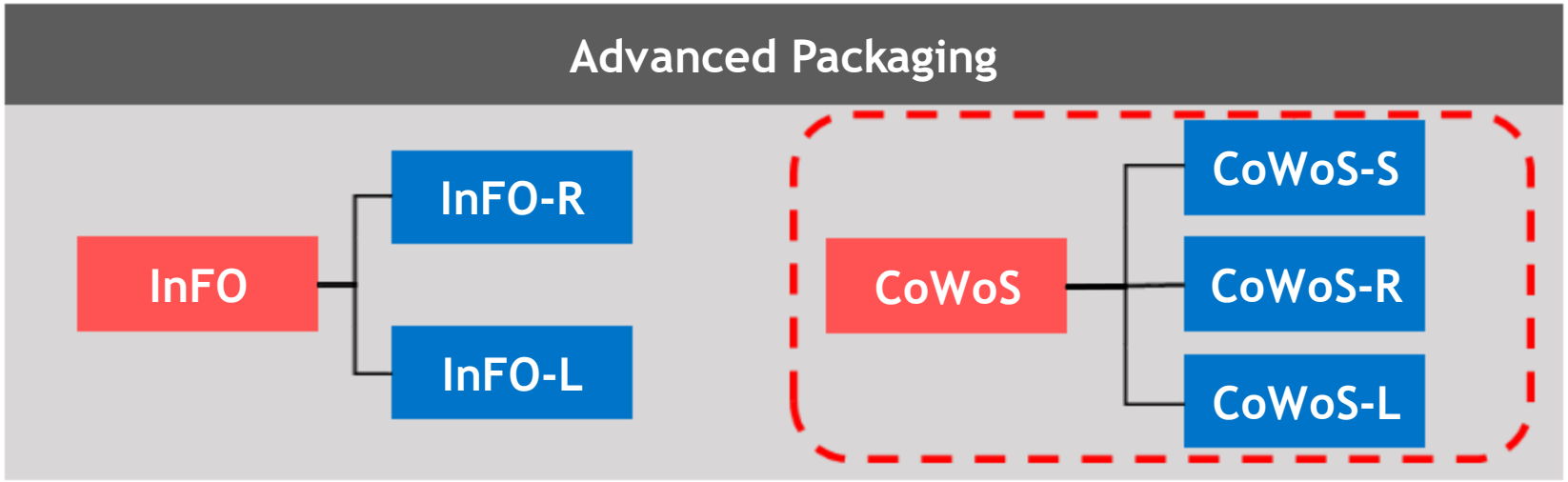
- SI/PI design-optimization at chip/interposer/package/board is demonstrated through this work, as well as electromagnetic simulation (Ansys HFSS, RaptorX, SIwave, Q2D) are employed at the design-optimization.



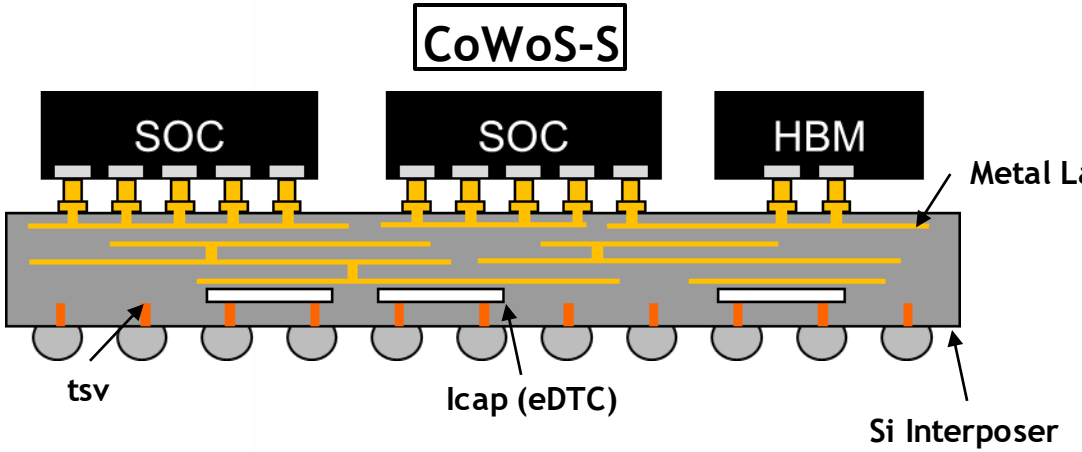
Silicon Proven

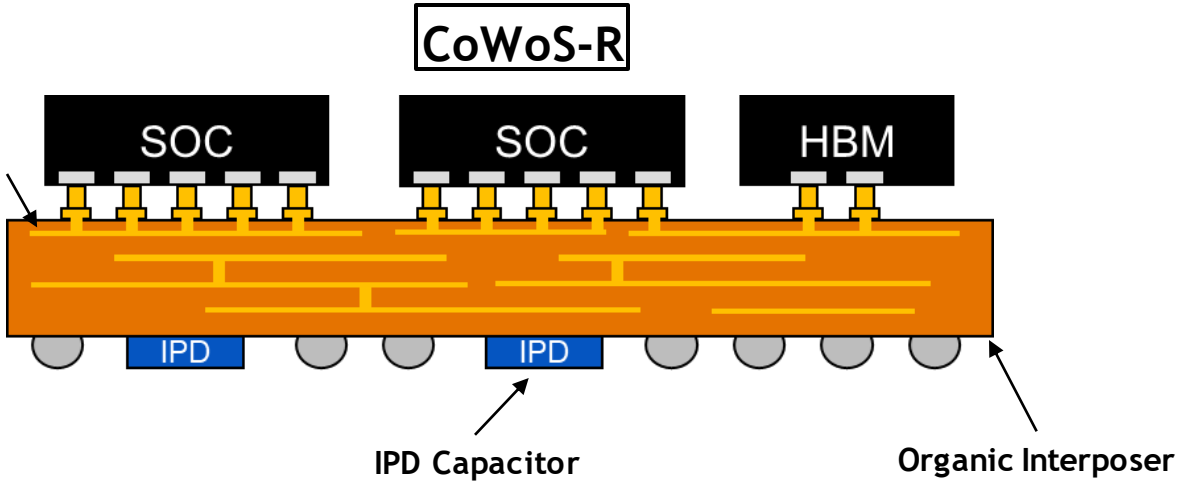


Decoupling Technology on APT



Current HBM Application

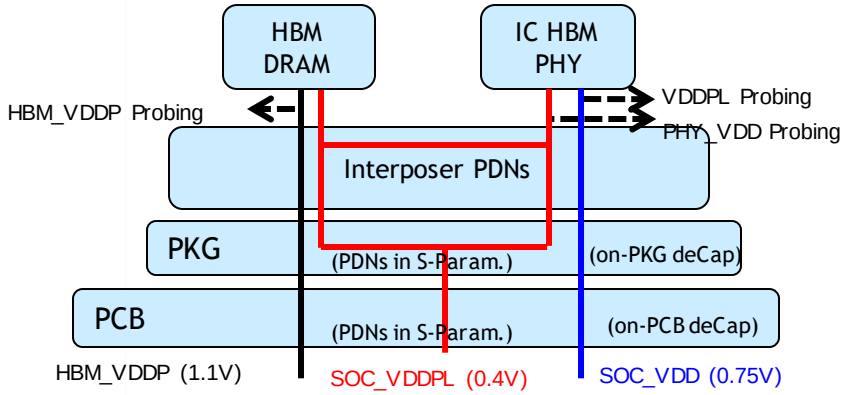




Power Integrity Co-design

Power Integrity Co-simulation topology

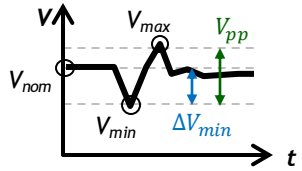
PHY Core power; PHY IO power + HBM Core/IO power



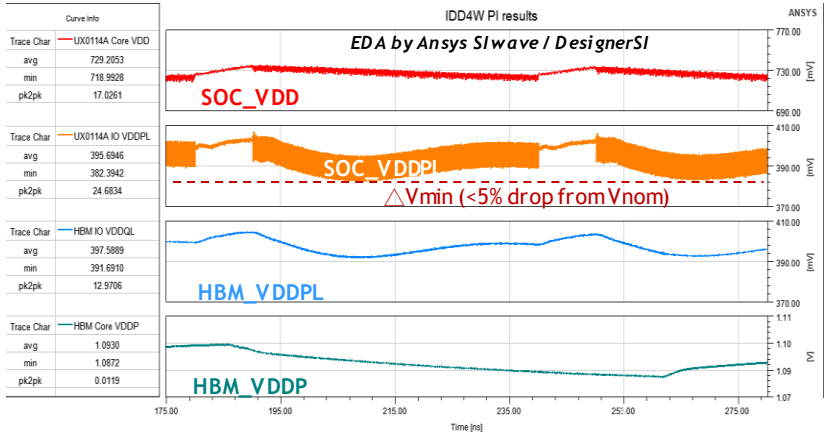
Interposer Types	HBM3 PHY Core & I/O Power Noises	Write Operation △Vmin		Read Operation △Vmin	
		DC-drop	AC-drop	DC-drop	AC-drop
CoWoS-S	HBM3 PHY Core Power (VDD=0.75V)	729.2mV (2.8%)	719mV (4.1%)	729.6mV (2.7%)	722.9mV (3.6%)
	HBM3 PHY I/O Power (VDDPL=0.4V)	395.7mV (1.1%)	382.4mV (4.4%)	396.8mV (0.8%)	391mV (2.3%)
CoWoS-R	HBM3 PHY Core Power (VDD=0.75V)	731.8mV (2.4%)	719.8mV (4.0%)	731.8mV (2.4%)	721.4mV (3.8%)
	HBM3 PHY I/O Power (VDDPL=0.4V)	398.2mV (0.5%)	382.1mV (4.5%)	398.4mV (0.4%)	391.7mV (2.1%)
Design Target for Power Integrity Co-sim./Sign-off		△Vmin < 5%	△Vmin < 5%	△Vmin < 5%	△Vmin < 5%

Simulation conditions

- CPM model : SOC_CPM + HBM_CPM
- PDN model : Interposer, PKG, PCB
- Simulation conditions including
  - IDD4W (SOC_CPM+ HBM_CPM)
  - IDD4R (SOC_CPM+ HBM_CPM)

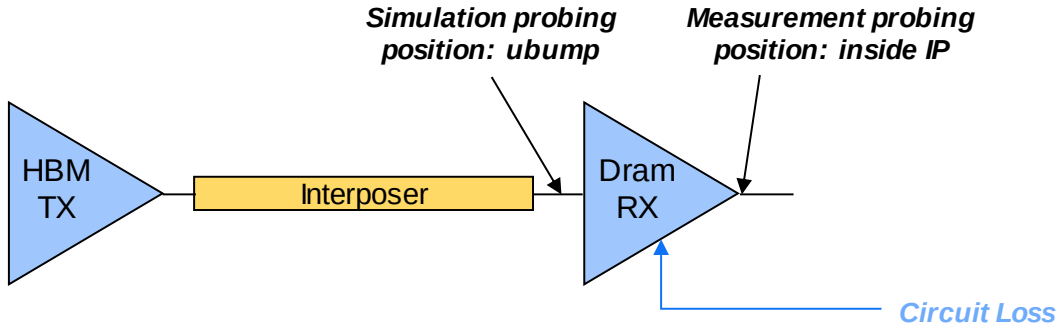


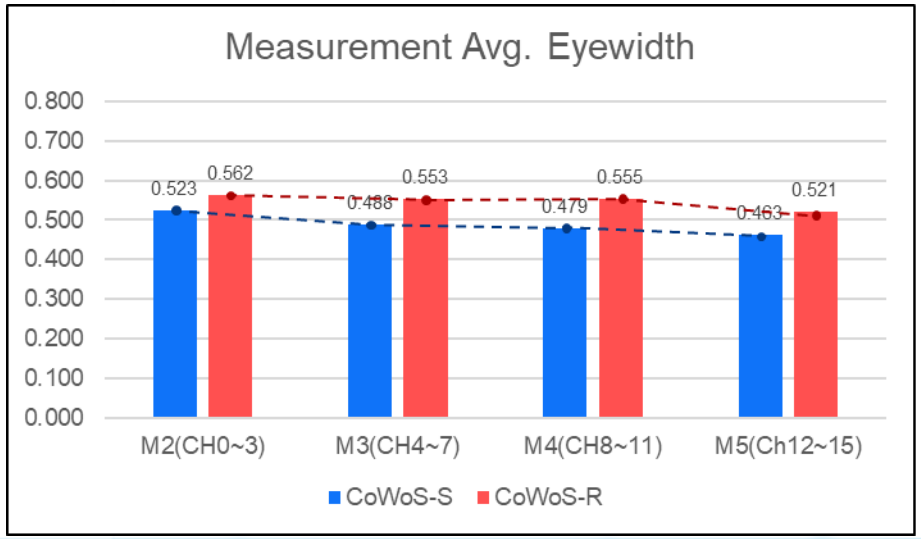
Power Integrity Co-sim., IDD4W- Zigzag @ CoWoS-S

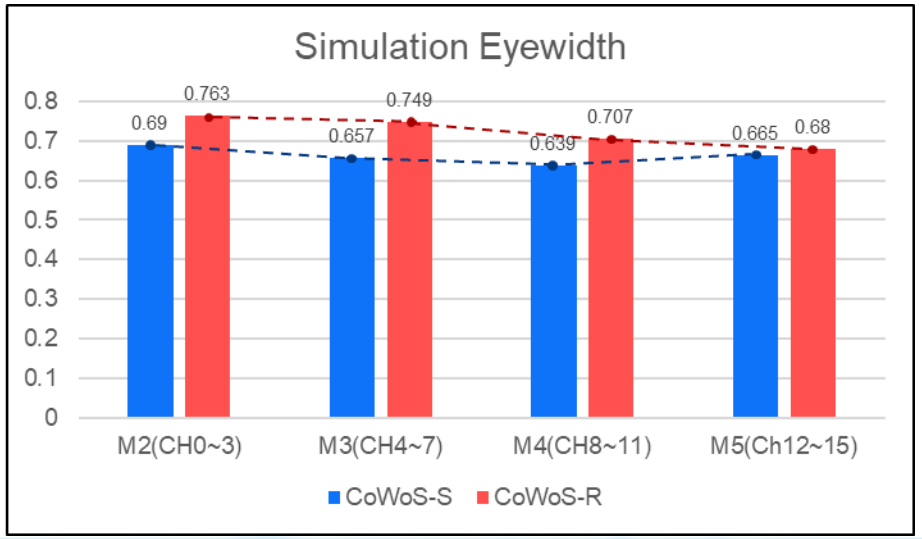


Write Operation Measurement Data and Simulation Correlation

- Interconnects co-simulated eyewidth at write pattern is 0.64-0.69UI at CoWoS-S, and 0.68-0.76UI at CoWoS-R, where measured eye-width is correlated with 0.46-0.56UI with around 20%(27ps) realistic circuit loss(Timing Skew/Jitter) in measurement.
  - Good correlation between simulation and measurement







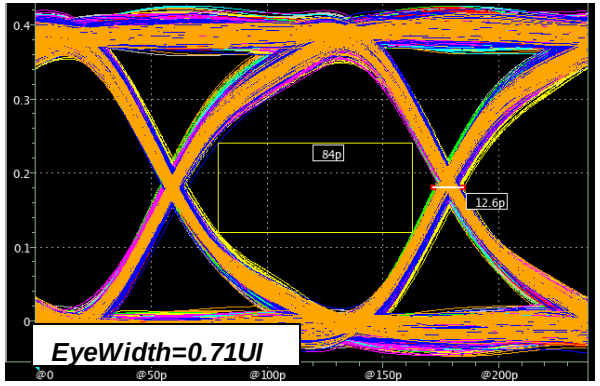
Summary

- This work presents an HBM3-7.2Gbps 2.5D-IC integration with signal and power integrity designs and silicon proven, which can provide up to 922 GB/s data bandwidth, implemented both at CoWoS-S and CoWoS-R.
  - Maximum voltage fluctuation can be suppressed by eDTC, IPD and on-PKG/PCB deCap to less than 5%, both at 0.4V & 0.75V power domains.
  - Interconnects co-simulated eyewidth at write pattern is 0.64-0.69UI at CoWoS-S, and 0.68-0.76UI at CoWoS-R, where measured eyewidth is correlated with 0.46-0.56UI with around 20% circuit loss.
    - Good correlation between simulation and measurement
- SI/PI design-optimization at chip/interposer/package/board is demonstrated through this work, as well as electromagnetic simulation (Ansys HFSS, RaptorX, SIwave, Q3D/Q2D) are employed at the design-optimization.
  - Signal Integrity designs at high speed interconnects for transmission performance.
  - Power Integrity designs at whole PDNs parasitics and decoupling capacitors deployment.

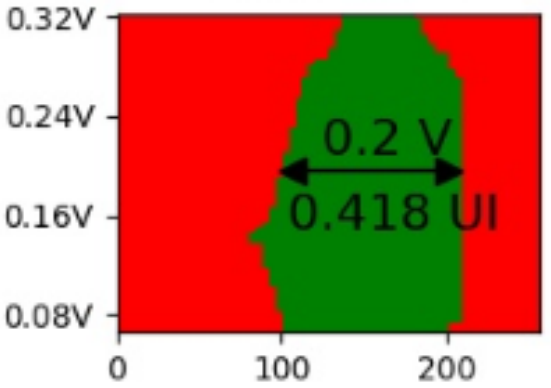
Recent Update

- The most recent update for HBM3 is with HBM3 IP PHY in 5nm, and CoWoS-S interposer in 65nm, it can achieve HBM3-8.4Gbps with silicon proven.

Simulation Sign-off



Silicon Proven



Thank you for your attention

Q&A Time